Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. Ea**
2. **A0a**
3. **A1a**
4. **N. O0a**
5. **N. O1a**
6. **N. O2a**
7. **N. O3a**
8. **GND**
9. **N. O3b**
10. **N. O2b**
11. **N. O1b**
12. **N. O0b**
13. **A1b**
14. **A0b**
15. **N. Eb**
16. **VCC**

**.059”**

**.058”**

**AC139**

**MASK**

**REF**

**14 13 12**

**11**

**10**

**9**

**8**

**7**

**3 4 5 6**

**15**

**16**

**16**

**1**

**2**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: AC139**

**APPROVED BY: DK DIE SIZE .058” X .059” DATE: 8/25/21**

**MFG: ON SEMI/MOTOROLA THICKNESS .012” P/N: 54AC139**

**DG 10.1.2**

#### Rev B, 7/19/02